

A Compact Self-similar Power Combining Topology

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Abstract—A compact, modular 16-way combiner is presented which is based on a self-similar combiner topology. The combiner achieves a simulated passive efficiency of 38% at 77 GHz in a standard 90nm process with 1.49 μm thick Al top metal. A 77 GHz power amplifier is built based on the combiner, combining the output power of 16 stages to achieve a P_{sat} of 11.4dBm, small signal gain of 9.4dB, and a 3dB bandwidth of more than 11 GHz on a 0.7V supply, with the optimal MAG for the technology being approximately 5dB at 77 GHz. The power amplifier is unconditionally stable with the K factor exceeding 3.8 between 50-90 GHz. The entire architecture is based on a modular power splitting and combining network that makes the design flexible and scalable. To the best of the authors' knowledge, this is the highest P_{sat} reported at 77 GHz in CMOS with a sub 1V quiescent V_{ds} .

Index Terms—CMOS, Millimeter wave, power amplifier, power combining, self-similar, 77 GHz.

I. INTRODUCTION

There has been a recent surge of interest in fully integrated systems in CMOS for mm-wave frequencies, with applications targeting wireless communication, vehicular radar, imaging and sensing. This has followed from a natural trend of transistor scaling and a consequential increasing f_t , f_{max} of devices in progressively smaller nodes, which has made once uncharted territory accessible to silicon ICs. In such a realization, the integrated power amplifier (PA) still remains the most challenging block because of low breakdown voltages and reliability issues like hot carrier injection (HCI) [1]. This fundamentally limits the maximum power that can be extracted from a single stage without sacrificing efficiency, gain, and stability. It therefore becomes inevitable that the output power of several stages must be combined in order to achieve the desired power level. Also since available gain is limited and ohmic losses are high at mm-wave frequencies, it becomes necessary to cascade several stages to boost up the power gain, often at the cost of efficiency.

In this paper, we present a scalable compact combiner topology which is based on a self-similar modular design. The design is an effort towards realizing the broader concept illustrated in Fig. 1 where the entire combiner network is similar to a part of itself. The output currents of four stages driven in phase combine with four similar output stages which again combine with four similar stages and the self-replication continues. Such self-similarity will not only make the design more modular, flexible and compact for lower loss, but will also make it more scalable than a more conventional

current combining corporate network where physical distance of separation between the stages increases rapidly with number of stages [2]. The symmetry of this design also ensures a symmetric thermal profile in the die which affects each of the 4-way combining stages in a similar way, unlike a conventional corporate combiner where the temperature rise experienced by the middle stages is higher. As a proof of concept, we present the design of a 16-way combiner which combines the power of 16 output stages to achieve a P_{sat} of +11.4dBm at 77 GHz on a 0.7 V supply. This is the highest reported P_{sat} in this frequency band in CMOS with a sub 1V supply, that is necessary for long term reliability of the devices.

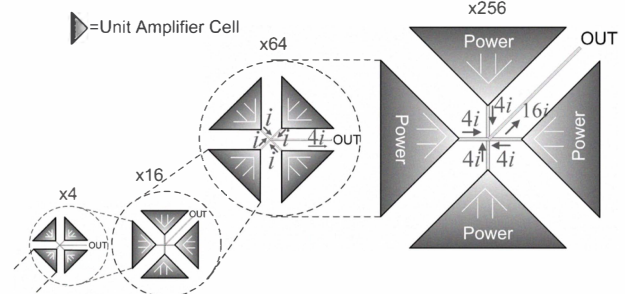


Fig. 1. A conceptual self-similar output combiner for combining currents from four output stages where each output stage is a scaled self-replicated version of the four output stages in an iterative way

II. POWER COMBINING

Given a technology, there is an optimum value of power which can be reliably obtained from a single stage without sacrificing power gain, stability and bandwidth. It is important to understand the trade-offs in order to appreciate the relevance of power combining.

A. Importance of Power Combining

When the transistor is operated at a frequency near its f_{max} , the gain is limited by the quality factor of its input impedance. The resistive part of this impedance which sinks the input RF power, is contributed by the resistance of the polysilicon, the gate contacts and also by the delayed trans-conductance caused due to the transit delay between the charge induction in the channel and the instantaneous gate voltage, commonly known as 'nonquasistatic' effect [3]. The quality factor and therefore, the power gain and f_{max} , can be increased by reducing the

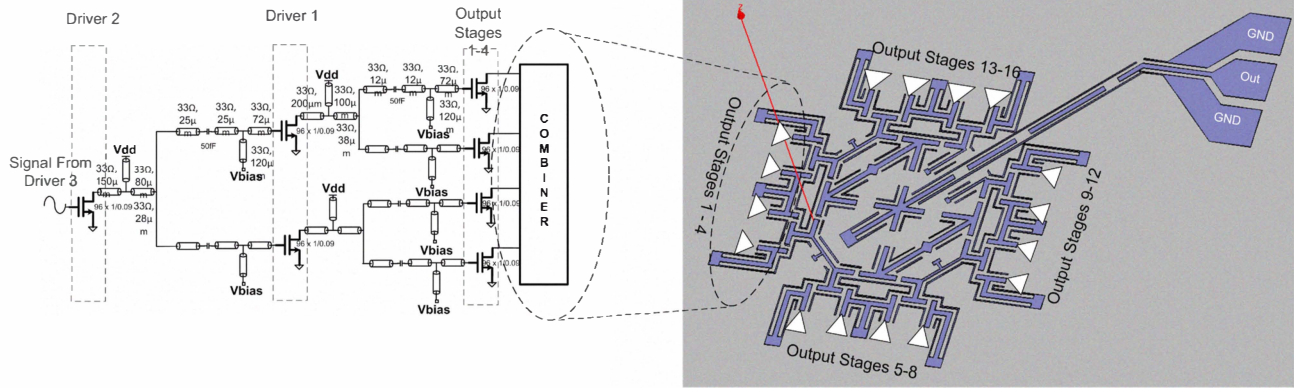


Fig. 2. Output combiner design for combining current from 16 output stages driven in phase. The combiner also achieves impedance transformation. The spaces in the transmission line network of the combiner represent ports where capacitors were placed as parts of the matching network. It also shows the schematic of the last three stages in each of the four arms of the combiner. It consists of Driver 1, Driver 2 and Output stage which have been illustrated in Fig. 4 and Fig. 5

gate width per finger until the transistor becomes unstable from the output port for a conjugate input match. Thus, for an optimum gate width per finger, the power gain of a transistor biased at its maximum f_{max} is fixed by technology. In this design, for a finger width of $1\mu m$, the MAG was 5dB at 77 GHz at a bias of $0.16mA/\mu m$.

For an optimal finger width and bias, the output voltage swing will be limited by the breakdown of the devices and the long term reliability issues like HCI and time-dependent dielectric breakdown. The device time to failure is exponential with the voltage swing and it is imperative to operate far away from this region. This fixes the supply voltage, which in this design is set at 0.7V. The output power, however, can be increased in theory by adding fingers in parallel and scaling down the desired output impedance for a proportionately higher current swing. In practice, such an optimistic scaling fails beyond a point primarily due to the following factors.

The low input and output impedance of a 'giant' output stage will imply a high impedance transformation ratio in the interstage as well as the output matching network leading to high loss and possible instability into the preceding stage [4]. This also reduces bandwidth and makes the design more sensitive to modeling errors. Also beyond a point, the connecting and feeding wiring resistance and inductance would overwhelm the benefit of adding irrationally large number of elements. In this technology, for a $96\mu m$ finger wide transistor, the saturated output power is around 5.5 dBm for a large signal load-pull match.

B. Efficient Power Combining

In order to increase the net output power, therefore, it is evident that power combining is necessary. Any loss in the output combiner, however, is critical and directly reduces efficiency and cannot be compensated for, unlike interstage losses. Assuming around 4 dB of combiner loss, around 16 output stages each delivering 5.5dBm need to be combined in order to generate +13dBm of output power. The problem of designing

a combiner to ensure maximum large signal power transfer to a 50Ω load through a lossy matching network is a multi-dimensional optimization procedure [1]. We know, however, that in silicon ICs, high-frequency loss is primarily dominated by metal loss due to storage of magnetic energy (as opposed to storage of electrical energy in the dielectric). Hence, in order to achieve a given inductive impedance transformation and store a given amount of net reactive energy, the average capacitive energy stored in the passive network has to be minimized, since any electrical energy needs to be compensated by an excess magnetic energy leading to higher loss. Ideally, therefore we should use only inductors with no capacitors to achieve the impedance transformation. However since inductors have finite self-resonant frequencies and transformer geometry also includes distributed capacitance, we use transmission lines in the combiner, splitter as well as in inter-stage matching networks. T-lines have predictable return paths and also scale up more readily with frequency. When a transmission line is terminated with a load of reflection coefficient, $|\Gamma_L| e^{j\theta}$, the average magnetic energy stored inside the line is given by $W_m = \frac{1}{2} \int_0^l L |I(x)|^2 dx = f(l, |\Gamma_L|, \theta)$ and the average electrical energy is given by $W_e = \frac{1}{2} \int_0^l C |V(x)|^2 dx = g(l, |\Gamma_L|, \theta)$ and the impedance transforming network with the highest W_m/W_e ratio will be the most efficient.

In this design, we combine the power of 16 such output stages driven in phase and current combine the output progressively through a modular matching network which realizes the power combining and impedance transformation at the same time. In order to minimize loss, and to make the layout compact, the combiner is made symmetrical and equidistant from 16 output stages as shown in Fig. 2. It has a binary tree-like structure and progressively adds current from the previous two stages finally adding 16 in phase currents in the center node. At each intersection point of the combiner, current gets added with the impedance looking into it doubled at each branch, while the combiner brings the impedance down

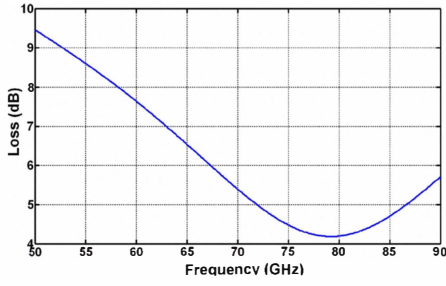


Fig. 3. Simulated loss (passive efficiency) of the combiner

again through a network of t-lines and capacitors to achieve the desired load-pull impedance. This approach leads to a combiner with a simulated passive efficiency of 38% at 77 GHz as shown in Fig. 3. Each of the feeding arms in the 16-way combiner is also fed through a series of self-similar driver amplifiers and matching networks as shown in Fig. 4 and explained in the next section. In theory, each such combiner can be self-replicated to make four such combiners combining the output power after having transformed the terminating 50Ω to 200Ω .

III. ARCHITECTURE AND AMPLIFIER DESIGN

The entire PA architecture, along with power splitting and combining, has been shown in Fig. 4. For the driver amplifiers typically, the transistors are sized in the ratio of 1:2 in a cascaded chain so that the output saturates when it has at least 3 dB of gain. Therefore the driver stages (each $48\mu\text{m}$) of two output stages (each $96\mu\text{m}$) can be combined into a single stage of width $96\mu\text{m}$. The same procedure can be carried out on the initial driver stages to enable a binary tree scaling. This concept is illustrated in Fig. 4 which shows the combining network and the self-similar active power splitting among different stages through transmission lines. In this way, a modular design methodology can be established and laying out separate optimized transistors and separate transformation networks for each stage can be avoided. However, layout constraints entail using slightly different matching network for different stages. The power flow among various branches at saturation is also shown in Fig. 4, assuming each stage has 3dB of gain at saturation and branches are lossless. Let P_{out} be the power delivered by each output stage consuming P_{DC} of DC power and let L be the combiner loss factor in the such a N cascaded binary corporate combiner [2](here $N = 5$). Then the drain efficiency (E_{nw}) of the entire network is given by

$$E_{nw} = \frac{L \sum_{i=0}^{2^N-1} P_{out}}{\sum_{i=0}^{N-1} 2^i P_{DC}} = \frac{L}{2} \frac{2^N}{2^N - 1} \frac{P_{out}}{P_{DC}} \approx \frac{1}{2} L E_{single} \quad (1)$$

where E_{single} is the drain efficiency of a single output stage. It can be seen that the efficiency gets reduced to less than

50% for such cascaded combiners; however such a reduction is unavoidable in order to achieve a higher saturation gain and a higher saturated output power.

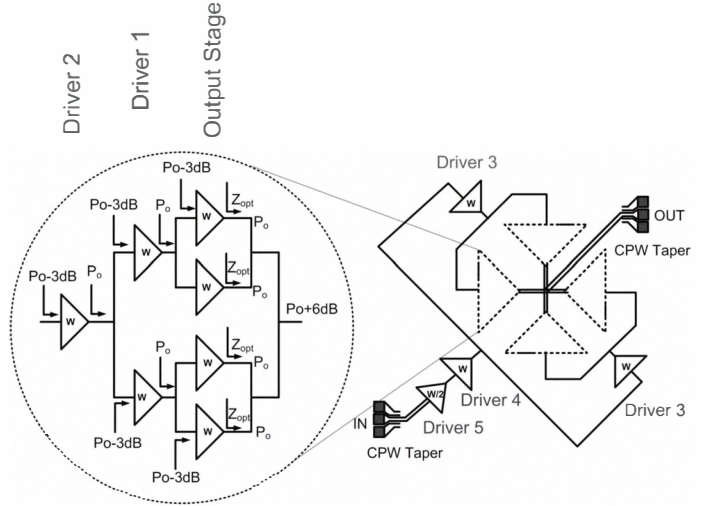


Fig. 4. The PA architecture showing the power splitting, combining networks and power flow among various branches at saturation assuming each stage has 3dB of saturated gain and branches are lossless

The whole network consists of six stages and the input transistors have a width $48\mu\text{m}$. Each 96 finger transistor is laid out as 8 parallel transistors, each of 12 fingers, to distribute the gate resistance and maximize gain ensuring minimum gate-drain side-wall capacitance for improved stability. The input and output CPW tapers are absorbed as parts of the matching network. All impedance transforming networks are designed using microstrip tub structure [1] with the $1.49\mu\text{m}$ thick top Al metal being used as the signal path. Spacing and width of the ground lines are optimized for loss and transmission line length. Although most of the return current is forced through the ground plane, the ground wall provides isolation necessary to make the combiner layout compact and low-loss. The schematic of the last three stages with detailed matching network is shown in Fig. 2.

Metal-oxide-Metal (MOM) capacitors were employed in the matching network and for bypass. Extensive 3D EM simulations (Ansoft HFSS) were performed to accurately predict self-resonance frequency (SRF) of the capacitors. A wide-band model (1-110 GHz) was then fitted which matched simulations within 0.5% over the entire frequency range. 200fF capacitors were simulated to resonate around 80 GHz. They were used in series with suitable resistors to achieve low impedance bypass.

IV. MEASUREMENT SET-UP AND RESULTS

The die microphotograph is shown in Fig. 5. The chip occupies an area of $1.3 \times 1.3 \text{ mm}^2$. Small-signal measurements are carried on wafer through WR-10 GSG Infinity probes connected to Agilent PNA 8361A through TX-RX modules. The Agilent 8316A vector network analyzer is calibrated using W-band calibration substrates since the pads have been

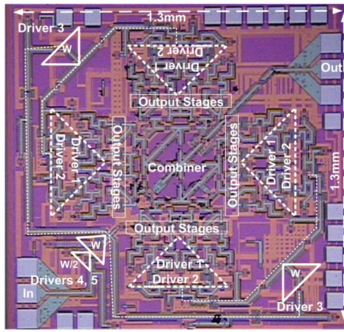


Fig. 5. Die microphotograph of the 77 GHz amplifier showing the layout placements of the different stages and the power splitting and combining network.

assimilated in the matching networks. The PA is biased in class AB mode and the DC current drawn is 472mA from a 0.7V supply. The measured small-signal parameters are shown in Fig. 6. The input match is below -19dB at 77 GHz and is below -10dB between 70-82 GHz. S_{22} is below -8dB at 77 GHz. The small signal gain of the amplifier is around 9.4 dB at 77GHz and has 3dB bandwidth between 72.5-83.5 GHz and has gain upto 87 GHz. No instability was observed and the measured K-factor is greater than 3.8 between 50-90 GHz.

The large signal performance of the PA at 77GHz is shown in Fig. 7. The input signal is provided through WR-10 GSG probes and attenuator using a quadrupler (Spaceklabs AE-4XW) which can deliver 12.3dBm output power at 77 GHz, enough to saturate the PA. The input signal at 19.25 GHz to the quadrupler was provided by Agilent 8257D. The output power was measured with W-band Agilent W8486A power sensor connected to Agilent 4418B power meter after de-embedding the probe loss. The PA has a saturation output power of 11.4 dBm and a saturated gain of 5dB. To the best of the authors' knowledge, the PA achieves the highest P_{sat} among reported work in CMOS at this frequency with a sub 1V quiescent V_{ds} , despite being implemented in a 90nm process with a relatively lower f_{max} compared to finer line processes used in other implementations [5]-[10]. In general, although higher P_{sat} and efficiency can be obtained by operating at higher supply voltages, it was kept low at 0.7V to operate far away from low breakdown and ensure long term reliability.

V. CONCLUSION

This paper presents a compact modular 16-way combiner based on a self-similar combiner topology. The combiner achieves a simulated passive efficiency of 38% at 77 GHz in a standard 90nm CMOS process with a 1.49 μ m thick Al top metal. A 77 GHz power amplifier is built based on the combiner which combines the output power of 16 stages to achieve a P_{sat} of 11.4dBm, small signal gain of 9.4dB, and a 3dB bandwidth of more than 11 GHz on a 0.7V supply, with the optimal MAG of the process being approximately 5dB at 77 GHz. The power amplifier is unconditionally stable with the K factor exceeding 3.8 between 50-90 GHz. The entire architecture is based on a modular power splitting and

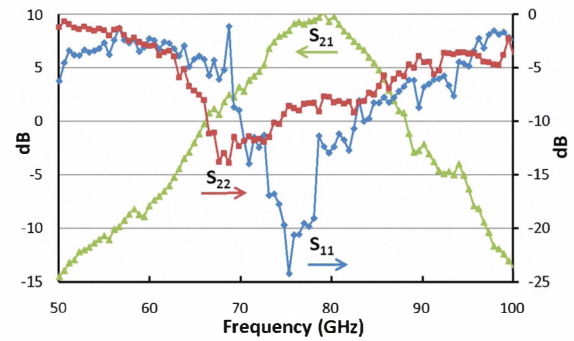


Fig. 6. Measured S-parameters of the power amplifier

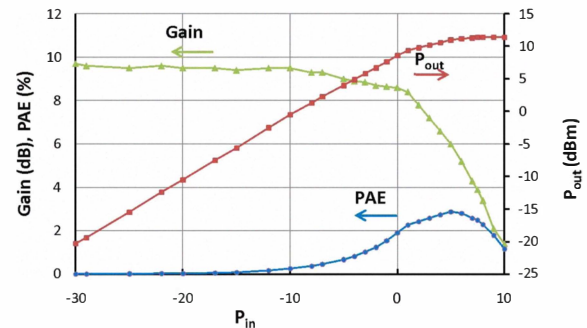


Fig. 7. Measured output power, gain and PAE at 77 GHz.

combining network that makes the design flexible and scalable. To the best of the authors' knowledge, this is the highest P_{sat} reported at 77 GHz in CMOS on a sub 1V quiescent V_{ds} . The supply was kept at a low voltage of 0.7V which is essential for PAs in deep submicron CMOS because of low breakdown and long term reliability issues.

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